

Lecture 11: Case Study— Tomasulo Algorithm

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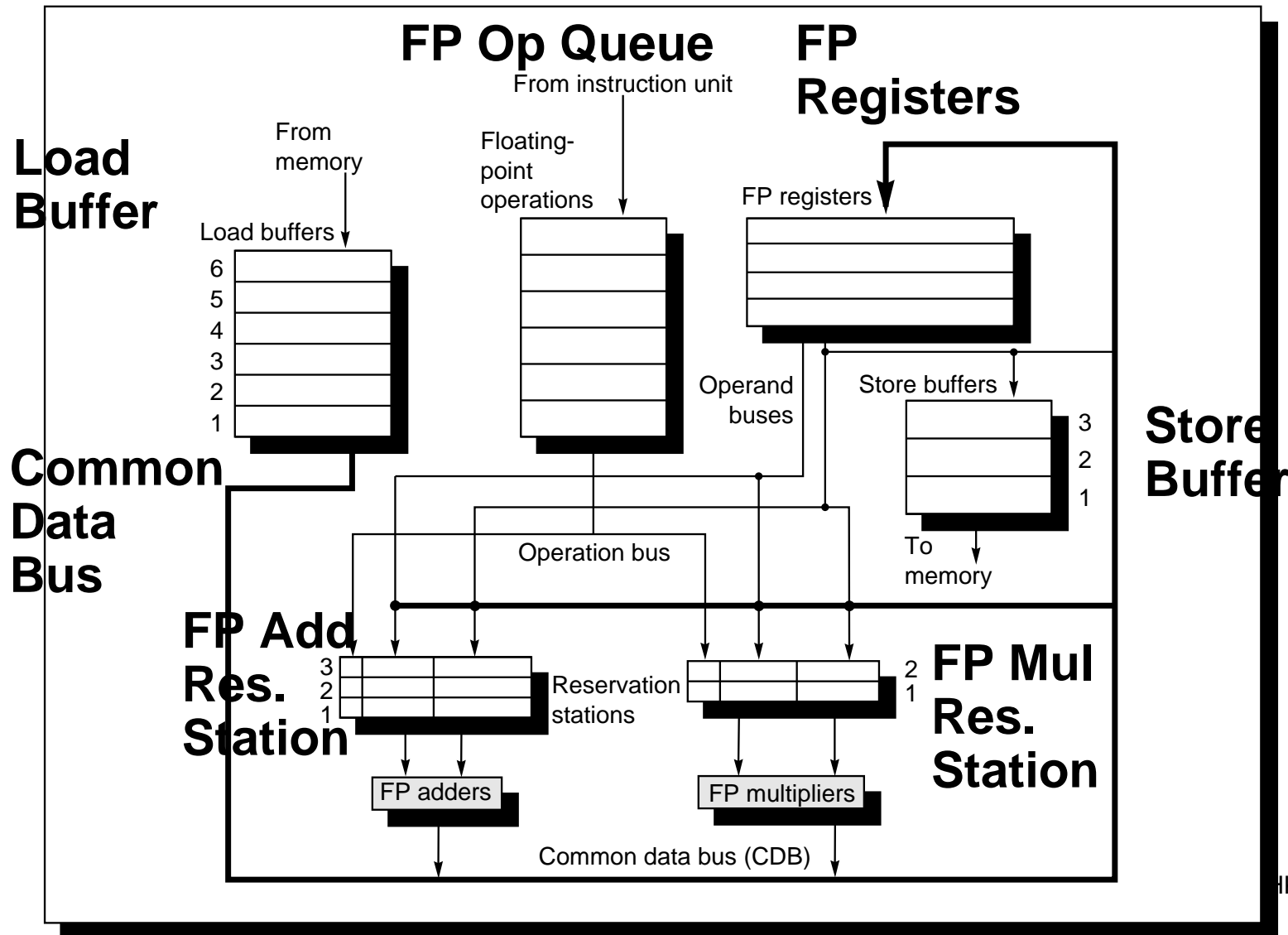
Review: Scoreboard Summary

- **Speedup 1.7 from compiler; 2.5 by hand
BUT slow memory (no cache)**
- **Limitations of 6600 scoreboard**
 - No forwarding
 - Limited to instructions in basic block (small *window*)
 - Number of functional units(structural hazards)
 - Wait for WAR hazards
 - Prevent WAW hazards

Another Dynamic Algorithm: Tomasulo Algorithm

- **For IBM 360/91 about 3 years after CDC 6600**
- **Goal: High Performance without special compilers**
- **Differences between IBM 360 & CDC 6600 ISA**
 - IBM has only 2 register specifiers/instr vs. 3 in CDC 6600
 - IBM has 4 FP registers vs. 8 in CDC 6600
- **Differences between Tomasulo Algorithm & Scoreboard**
 - Control & buffers distributed with Function Units vs. centralized in scoreboard; called “reservation stations”
 - Registers in instructions replaced by pointers to reservation station buffer
 - HW renaming of registers to avoid WAR, WAW hazards
 - Common Data Bus broadcasts results to all FUs
 - Load and Stores treated as FUs as well

Tomasulo Organization



Reservation Station Components

Op—Operation to perform in the unit (e.g., + or −)

Qj, Qk—Reservation stations producing source registers

Vj, Vk—Value of Source operands

Rj, Rk—Flags indicating when Vj, Vk are ready

Busy—Indicates reservation station and FU is busy

Register result status—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions that will write that register.

Three Stages of Tomasulo Algorithm

1. Issue—get instruction from FP Op Queue

If reservation station free, the scoreboard issues instr & sends operands (renames registers).

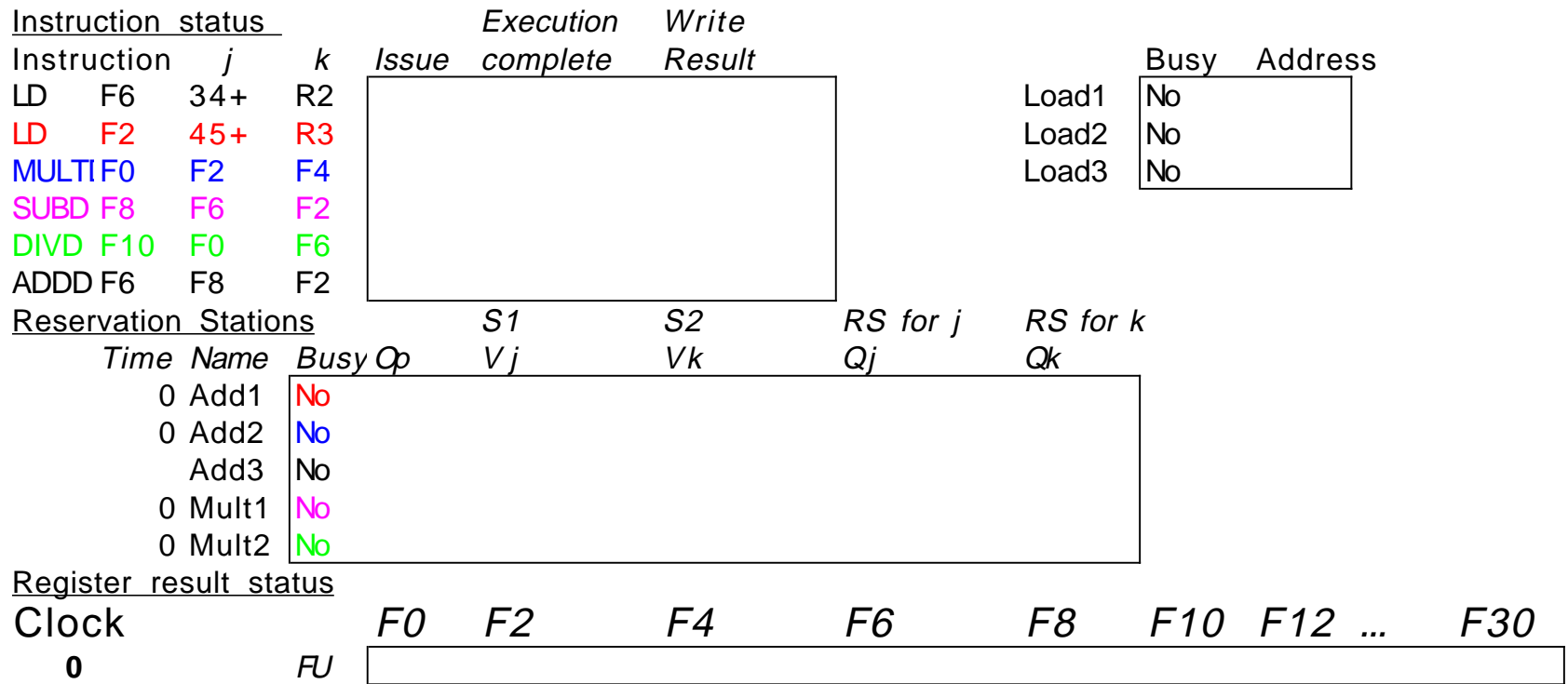
2. Execution—operate on operands (EX)

When both operands ready then execute;
if not ready, watch CDB for result

3. Write result—finish execution (WB)

Write on Common Data Bus to all awaiting units;
mark reservation station available.

Tomasulo Example Cycle 0



Tomasulo Example Cycle 1

<u>Instruction status</u>				<i>Execution</i>	<i>Write</i>		
Instruction	<i>j</i>	<i>k</i>	<i>Issue</i>	<i>complete</i>	<i>Result</i>	Busy	Address
LD	F6	34+	R2	1		Load1	No 34+R2
LD	F2	45+	R3		Load2	No	
MULTI	F0	F2	F4		Load3	No	
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

<u>Reservation Stations</u>			<i>S1</i>	<i>S2</i>	<i>RS for j</i>	<i>RS for k</i>
<i>Time</i>	<i>Name</i>	<i>Busy Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	No				
0	Mult2	No				

<u>Register result status</u>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
Clock	<i>FU</i>				Load1					
1										

Tomasulo Example Cycle 2

<u>Instruction status</u>				<i>Execution</i>	<i>Write</i>		
Instruction	<i>j</i>	<i>k</i>	<i>Issue</i>	<i>complete</i>	<i>Result</i>	Busy	Address
LD	F6	34+	R2	1		Load1	Yes 34+R2
LD	F2	45+	R3	2		Load2	Yes 45+R3
MULT	F0	F2	F4			Load3	No
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

<u>Reservation Stations</u>			<i>S1</i>	<i>S2</i>	<i>RS for j</i>	<i>RS for k</i>
<i>Time</i>	<i>Name</i>	<i>Busy Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	No				
0	Mult2	No				

<u>Register result status</u>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
Clock										
2	<i>FU</i>		Load2		Load1					

Tomasulo Example Cycle 3

Instruction status				Issue	Execution complete	Write Result	Load	Busy	Address
Instruction	<i>j</i>	<i>k</i>							
LD	F6	34+	R2	1	3		Load1	Yes	34+R2
LD	F2	45+	R3	2			Load2	Yes	45+R3
MULTI	F0	F2	F4	3			Load3	No	
SUBD	F8	F6	F2						
DIVD	F10	F0	F6						
ADDD	F6	F8	F2						

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	Yes MULTD		R(F4)	Load2	
0	Mult2	No				

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
3	FU	Mult1	Load2		Load1					

Tomasulo Example Cycle 4

Instruction status				Issue	Execution complete	Write Result	Load	Busy	Address
Instruction	<i>j</i>	<i>k</i>							
LD	F6	34+	R2	1	3	4	Load1	No	
LD	F2	45+	R3	2			Load2	Yes	45+R3
MULTI	F0	F2	F4	3			Load3	No	
SUBD	F8	F6	F2	4					
DIVD	F10	F0	F6						
ADDD	F6	F8	F2						

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	Yes SUBD	M(34+R2)			Load2
0	Add2	No				
	Add3	No				
0	Mult1	Yes MULTD		R(F4)	Load2	
0	Mult2	No				

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
4	FU	Mult1	Load2		M(34+R2)	Add1				

Tomasulo Example Cycle 5

Instruction status				Issue	Execution complete	Write Result	Load	Busy	Address
Instruction	<i>j</i>	<i>k</i>							
LD	F6	34+	R2	1	3	4	Load1	No	
LD	F2	45+	R3	2	5		Load2	Yes	45+R3
MULTI	F0	F2	F4	3			Load3	No	
SUBD	F8	F6	F2	4					
DIVD	F10	F0	F6	5					
ADDD	F6	F8	F2						

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	Yes SUBD	M(34+R2)			Load2
0	Add2	No				
	Add3	No				
0	Mult1	Yes MULTD		R(F4)	Load2	
0	Mult2	Yes DIVD		M(34+R2)	Mult1	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
5	FU	Mult1	Load2		M(34+R2)	Add1	Mult2			

Tomasulo Example Cycle 6

Instruction status				Execution	Write			
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result	Busy	Address	
LD	F6	34+	R2	1	3	4	Load1	No No No
LD	F2	45+	R3	2	5	6	Load2	
MULTI	F0	F2	F4	3			Load3	
SUBD	F8	F6	F2	4				
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6				

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
2	Add1	Yes	SUBD	M(34+R2)	M(45+R3)	
0	Add2	Yes	ADDD		M(45+R3)	Add1
	Add3	No				
10	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD		M(34+R2)	Mult1

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	6	Mult1	M(45+R3)		Add2	Add1	Mult2			

Tomasulo Example Cycle 7

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4				
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6				

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
1	Add1	Yes	SUBD	M(34+R2)	M(45+R3)	
0	Add2	Yes	ADDD		M(45+R3)	Add1
	Add3	No				
9	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD		M(34+R2)	Mult1

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	7	FU	Mult1	M(45+R3)	Add2	Add1	Mult2			

Tomasulo Example Cycle 8

Instruction status				Issue	Execution complete	Write Result		Busy	Address
Instruction	<i>j</i>	<i>k</i>							
LD	F6	34+	R2	1	3	4		Load1	No
LD	F2	45+	R3	2	5	6		Load2	No
MULTI	F0	F2	F4	3				Load3	No
SUBD	F8	F6	F2	4	8				
DIVD	F10	F0	F6	5					
ADDD	F6	F8	F2	6					

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	Yes	SUBD	M(34+R2)	M(45+R3)	
0	Add2	Yes	ADDD		M(45+R3)	Add1
	Add3	No				
8	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD	M(34+R2)		Mult1

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
8	FU	Mult1	M(45+R3)		Add2	Add1	Mult2			

Tomasulo Example Cycle 9

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6				

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	Yes	ADDD	M()-M()	M(45+R3)	
	Add3	No				
7	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD	M(34+R2)	Mult1	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	9	Mult1	M(45+R3)		Add2	M()-M()	Mult2			

Tomasulo Example Cycle 10

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6				

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
2	Add2	Yes	ADDD	M()-M()	M(45+R3)	
	Add3	No				
7	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD		M(34+R2)	Mult1

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
10	FU	Mult1	M(45+R3)		Add2	M()-M()	Mult2			

Tomasulo Example Cycle 11

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6				

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
1	Add2	Yes	ADDD	M()-M()	M(45+R3)	
	Add3	No				
5	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD	M(34+R2)	Mult1	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
11	FU	Mult1	M(45+R3)		Add2	M()-M()	Mult2			

Tomasulo Example Cycle 12

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12			

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	Yes	ADDD	M()-M()	M(45+R3)	
	Add3	No				
4	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD	M(34+R2)	Mult1	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
12	FU	Mult1	M(45+R3)		Add2	M()-M()	Mult2			

Tomasulo Example Cycle 13

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12	13		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
3	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD	M(34+R2)	Mult1	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
13	FU	Mult1	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 14

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12	13		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
2	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD		M(34+R2)	Mult1

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
14	FU	Mult1	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 15

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3			Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12	13		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
1	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD		M(34+R2)	Mult1

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
15	FU	Mult1	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 16

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3	16		Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12	13		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	Yes	MULTD	M(45+R3)	R(F4)	
0	Mult2	Yes	DIVD		M(34+R2)	Mult1

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
16	FU	Mult1	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 17

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3	16	17	Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12	13		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	No				
0	Mult2	Yes	DIVD	M*F4		M(34+R2)

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
17	FU	M*F4	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 18

<u>Instruction status</u>				<i>Execution</i>	<i>Write</i>		<i>Busy</i>	<i>Address</i>
Instruction	<i>j</i>	<i>k</i>	<i>Issue</i>	<i>complete</i>	<i>Result</i>			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3	16	17	Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12	13		

<u>Reservation Stations</u>			<i>S1</i>	<i>S2</i>	<i>RS for j</i>	<i>RS for k</i>
<i>Time</i>	<i>Name</i>	<i>Busy Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	No				
40	Mult2	Yes	DIVD	M*F4		M(34+R2)

<u>Register result status</u>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
Clock										
18	<i>FU</i>	M*F4	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 57

<u>Instruction status</u>				<i>Execution</i>	<i>Write</i>		<i>Busy</i>	<i>Address</i>
Instruction	<i>j</i>	<i>k</i>	<i>Issue</i>	<i>complete</i>	<i>Result</i>			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3	16	17	Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5				
ADDD	F6	F8	F2	6	12	13		

<u>Reservation Stations</u>			<i>S1</i>	<i>S2</i>	<i>RS for j</i>	<i>RS for k</i>
<i>Time</i>	<i>Name</i>	<i>Busy Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	No				
1	Mult2	Yes	DIVD	M*F4		M(34+R2)

<u>Register result status</u>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
57	<i>FU</i>	M*F4	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 58

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3	16	17	Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5	58			
ADDD	F6	F8	F2	6	12	13		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	No				
0	Mult2	Yes	DIVD	M*F4		M(34+R2)

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
58	FU	M*F4	M(45+R3)		(M-M)+M()	M()-M()	Mult2			

Tomasulo Example Cycle 59

Instruction status				Execution	Write		Busy	Address
Instruction	<i>j</i>	<i>k</i>	Issue	complete	Result			
LD	F6	34+	R2	1	3	4	Load1	No
LD	F2	45+	R3	2	5	6	Load2	No
MULTI	F0	F2	F4	3	16	17	Load3	No
SUBD	F8	F6	F2	4	8	9		
DIVD	F10	F0	F6	5	58	59		
ADDD	F6	F8	F2	6	12	13		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>
0	Add1	No				
0	Add2	No				
	Add3	No				
0	Mult1	No				
0	Mult2	No				

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
59	FU	M*F4	M(45+R3)		(M-M)+M()	M()-M()	M*F4/M			

Tomasulo Loop Example

Loop: LD	F0	0	R1
MULTD	F4	F0	F2
SD	F4	0	R1
SUBI	R1	R1	#8
BNEZ	R1	Loop	

- Multiply takes 4 clocks
- Load have cache misses

Loop Example Cycle 0

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Load1	Load2	Load3
LD	F0	0 R1	1				No	No	No
MULTI	F4	F0 F2	1				No	No	Qi
SD	F4	0 R1	1				No	No	
LD	F0	0 R1	2				No	No	
MULTI	F4	F0 F2	2				No	No	
SD	F4	0 R1	2				No	No	

Reservation Stations			S1	S2	RS for j	RS for k	Code:
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	No					SUBI R1 R1 # 8
0	Mult2	No					BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
0	80	Qi								

Loop Example Cycle 1

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Load	Address	
LD	F0	0 R1	1	1			Load1	Yes 80	
MULTI	F4	F0 F2	1				Load2	No	
SD	F4	0 R1	1				Load3	No Qi	
LD	F0	0 R1	2				Store1	No	
MULTI	F4	F0 F2	2				Store2	No	
SD	F4	0 R1	2				Store3	No	

Reservation Stations			S1	S2	RS for j	RS for k	Code:
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	No					SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
1	80	Qi	Load1							

Loop Example Cycle 2

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1		Load1	Yes	80	
MULTI	F4	F0 F2	1	2		Load2	No		
SD	F4	0 R1	1			Load3	No	Qi	
LD	F0	0 R1	2			Store1	No		
MULTI	F4	F0 F2	2			Store2	No		
SD	F4	0 R1	2			Store3	No		

Reservation Stations			S1	S2	RS for j	RS for k	Code:
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load1		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
2	80	Qi	Load1	Mult1						

Loop Example Cycle 3

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1		Load1	Yes	80	
MULTI	F4	F0 F2	1	2		Load2	No		
SD	F4	0 R1	1	3		Load3	No	Qi	
LD	F0	0 R1	2			Store1	Yes	80	
MULTI	F4	F0 F2	2			Store2	No	Mult1	
SD	F4	0 R1	2			Store3	No		

Reservation Stations			S1	S2	RS for j	RS for k	Code:
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load1		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
3	80	Qi	Load1	Mult1						

Loop Example Cycle 4

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1		Load1	Yes	80	
MULTI	F4	F0 F2	1	2		Load2	No		
SD	F4	0 R1	1	3		Load3	No	Qi	
LD	F0	0 R1	2			Store1	Yes	80	
MULTI	F4	F0 F2	2			Store2	No	Mult1	
SD	F4	0 R1	2			Store3	No		

Reservation Stations			S1	S2	RS for	RS for	k	Code:
Time	Name	Busy Op	Vj	Vk	Qj	Qk		
0	Add1	No						LD F0 0 R1
0	Add2	No						MULTI F4 F0 F2
0	Add3	No						SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load1			SUBI R1 R1 #8
0	Mult2	No						BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
4	72	Qi	Load1	Mult1						

Loop Example Cycle 5

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1		Load1	Yes	80	
MULTI	F4	F0 F2	1	2		Load2	No		
SD	F4	0 R1	1	3		Load3	No	Qi	
LD	F0	0 R1	2			Store1	Yes	80	
MULTI	F4	F0 F2	2			Store2	No	Mult1	
SD	F4	0 R1	2			Store3	No		

Reservation Stations			S1	S2	RS for j	RS for k	Code:
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load1		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
5	72	Qi	Load1	Mult1						

Loop Example Cycle 6

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1		Load1	Yes	80	
MULTI	F4	F0 F2	1	2		Load2	Yes	72	
SD	F4	0 R1	1	3		Load3	No	Qi	
LD	F0	0 R1	2	6		Store1	Yes	80	
MULTI	F4	F0 F2	2			Store2	No		
SD	F4	0 R1	2			Store3	No		
Reservation Stations				S1	S2	RS for	RS for	k	
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:	
0	Add1	No						LD F0 0 R1	
0	Add2	No						MULTI F4 F0 F2	
0	Add3	No						SD F4 0 R1	
0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI R1 R1 #8	
0	Mult2	No						BNEZ R1 Loop	
Register result status									
Clock	R1		F0	F2	F4	F6	F8	F10 F12... F30	
6	72	Qi	Load1	Mult1					

Loop Example Cycle 7

Instruction status				Execution Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1		Load1	Yes	80	
MULTI	F4	F0 F2	1	2		Load2	Yes	72	
SD	F4	0 R1	1	3		Load3	No	Qi	
LD	F0	0 R1	2	6		Store1	Yes	80	
MULTI	F4	F0 F2	2	7		Store2	No		
SD	F4	0 R1	2			Store3	No		

Reservation Stations			S1	S2	RS for	RS for	k
Time	Name	Busy Op	Vj	Vk	Qj	Qk	Code:
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load1		SUBI R1 R1 #8
0	Mult2	Yes	MULTD	R(F2)	Load2		BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
7	72	Qi	Load2	Mult2						

Loop Example Cycle 8

Instruction status				Execution Write			Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address
LD	F0	0 R1	1	1		Load1	Yes	80
MULTI	F4	F0 F2	1	2		Load2	Yes	72
SD	F4	0 R1	1	3		Load3	No	Q_i
LD	F0	0 R1	2	6		Store1	Yes	80
MULTI	F4	F0 F2	2	7		Store2	Yes	72
SD	F4	0 R1	2	8		Store3	No	

Reservation Stations			$S1$	$S2$	RS for j	RS for k	Code:
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes MULTD		R(F2)	Load1		SUBI R1 R1 #8
0	Mult2	Yes MULTD		R(F2)	Load2		BNEZ R1 Loop

Register result status			$F0$	$F2$	$F4$	$F6$	$F8$	$F10$	$F12$...	$F30$
Clock	R1										
8	72	Q_i	Load2	Mult2							

Loop Example Cycle 9

Instruction status				Execution			Write		Busy Address	
Instruction	j	k	iteration	Issue	complete	Result				
LD	F0	0 R1	1	1	9	Load1	Yes	80		
MULTI	F4	F0 F2	1	2		Load2	Yes	72		
SD	F4	0 R1	1	3		Load3	No			Qi
LD	F0	0 R1	2	6		Store1	Yes	80	Mult1	
MULTI	F4	F0 F2	2	7		Store2	Yes	72	Mult2	
SD	F4	0 R1	2	8		Store3	No			

Reservation Stations			S1	S2	RS for	RS for	k	Code:	
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k			
0	Add1	No							LD F0 0 R1
0	Add2	No							MULTI F4 F0 F2
0	Add3	No							SD F4 0 R1
0	Mult1	Yes	MULTD		R(F2)	Load1			SUBI R1 R1 # 8
0	Mult2	Yes	MULTD		R(F2)	Load2			BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
9	64	Qi	Load2		Mult2					

Loop Example Cycle 10

Instruction status				Execution Write			Busy Address	
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address
LD	F0	0 R1	1	1	9	10	Load1	No
MULTI	F4	F0 F2	1	2			Load2	Yes 72
SD	F4	0 R1	1	3			Load3	No Qi
LD	F0	0 R1	2	6	10		Store1	Yes 80 Mult1
MULTI	F4	F0 F2	2	7			Store2	Yes 72 Mult2
SD	F4	0 R1	2	8			Store3	No

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
4	Mult1	Yes MULTD	M(80)	R(F2)			SUBI R1 R1 #8
0	Mult2	Yes MULTD		R(F2)	Load2		BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
10	64	Qi	Load2	Mult2						

Loop Example Cycle 11

Instruction status				Execution			Write		
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1	9	10	Load1	No	
MULTI	F4	F0 F2	1	2			Load2	No	
SD	F4	0 R1	1	3			Load3	Yes	64 Qi
LD	F0	0 R1	2	6	10	11	Store1	Yes	80 Mult1
MULTI	F4	F0 F2	2	7			Store2	Yes	72 Mult2
SD	F4	0 R1	2	8			Store3	No	

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
3	Mult1	Yes MULTD	M(80)	R(F2)			SUBI R1 R1 #8
4	Mult2	Yes MULTD	M(72)	R(F2)			BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
11	64 Qi			Mult2						

Loop Example Cycle 12

Instruction status				Execution			Write		
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1	9	10	No		
MULTI	F4	F0 F2	1	2			No		
SD	F4	0 R1	1	3			Yes	64	Qi
LD	F0	0 R1	2	6	10	11	Yes	80	Mult1
MULTI	F4	F0 F2	2	7			Yes	72	Mult2
SD	F4	0 R1	2	8			No		

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
2	Mult1	Yes MULTD	M(80)	R(F2)			SUBI R1 R1 #8
3	Mult2	Yes MULTD	M(72)	R(F2)			BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
12	64 Qi			Mult2						

Loop Example Cycle 13

Instruction status				Execution			Write		
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1	9	10	Load1	No	
MULTI	F4	F0 F2	1	2			Load2	No	
SD	F4	0 R1	1	3			Load3	Yes	64 Qi
LD	F0	0 R1	2	6	10	11	Store1	Yes	80 Mult1
MULTI	F4	F0 F2	2	7			Store2	Yes	72 Mult2
SD	F4	0 R1	2	8			Store3	No	

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
1	Mult1	Yes MULTD	M(80)	R(F2)			SUBI R1 R1 #8
2	Mult2	Yes MULTD	M(72)	R(F2)			BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
13	64 Qi			Mult2						

Loop Example Cycle 14

Instruction status				Execution			Write		
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1	9	10	No		
MULTI	F4	F0 F2	1	2	14		No		
SD	F4	0 R1	1	3			Yes	64	Qi
LD	F0	0 R1	2	6	10	11	Yes	80	Mult1
MULTI	F4	F0 F2	2	7			Yes	72	Mult2
SD	F4	0 R1	2	8			No		

Reservation Stations			S1	S2	RS for j	RS for k	Code:
Time	Name	Busy Op	V_j	V_k	Q_j	Q_k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes MULTD	M(80)	R(F2)			SUBI R1 R1 #8
1	Mult2	Yes MULTD	M(72)	R(F2)			BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
14	64	Qi			Mult2					

Loop Example Cycle 15

Instruction status				Execution			Write		
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1	9	10	Load1	No	
MULTI	F4	F0 F2	1	2	14	15	Load2	No	
SD	F4	0 R1	1	3			Load3	Yes	64 Qi
LD	F0	0 R1	2	6	10	11	Store1	Yes	80 M(80)*R(
MULTI	F4	F0 F2	2	7	15		Store2	Yes	72 Mult2
SD	F4	0 R1	2	8			Store3	No	

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _{<i>j</i>}	V _{<i>k</i>}	Q _{<i>j</i>}	Q _{<i>k</i>}	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	No					SUBI R1 R1 #8
0	Mult2	Yes	MULTD	M(72) R(F2)			BNEZ R1 Loop

Register result status		F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1								
15	64 Qi			Mult2					

Loop Example Cycle 16

Instruction status				Execution			Write		
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0 R1	1	1	9	10	Load1	No	
MULT	F4	F0 F2	1	2	14	15	Load2	No	
SD	F4	0 R1	1	3			Load3	Yes	64 Qi
LD	F0	0 R1	2	6	10	11	Store1	Yes	80 M(80)*R1
MULT	F4	F0 F2	2	7	15	16	Store2	Yes	72 M(72)*R1
SD	F4	0 R1	2	8			Store3	No	

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULT F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load3		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status			F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1									
16	64	Qi	Mult1							

Loop Example Cycle 17

Instruction status				Execution			Write		Busy Address	
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result				
LD	F0	0 R1	1	1	9	10	Load1	No		
MULTI	F4	F0 F2	1	2	14	15	Load2	No		
SD	F4	0 R1	1	3			Load3	Yes	64	Qi
LD	F0	0 R1	2	6	10	11	Store1	Yes	80	M(80)*R(
MULTI	F4	F0 F2	2	7	15	16	Store2	Yes	72	M(72)*R(
SD	F4	0 R1	2	8			Store3	Yes	64	Mult1

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load3		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status		F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1								
17	64 Qi	Mult1							

Loop Example Cycle 18

Instruction status				Execution			Write		Busy Address	
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result				
LD	F0	0 R1	1	1	9	10	Load1	No		
MULTI	F4	F0 F2	1	2	14	15	Load2	No		
SD	F4	0 R1	1	3	18		Load3	Yes	64 Qi	
LD	F0	0 R1	2	6	10	11	Store1	Yes	80 M(80)*R(
MULTI	F4	F0 F2	2	7	15	16	Store2	Yes	72 M(72)*R(
SD	F4	0 R1	2	8			Store3	Yes	64 Mult1	

Reservation Stations			S1	S2	RS for	RS for	k	
Time	Name	Busy Op	Vj	Vk	Qj	Qk		Code:
0	Add1	No						LD F0 0 R1
0	Add2	No						MULTI F4 F0 F2
0	Add3	No						SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load3			SUBI R1 R1 #8
0	Mult2	No						BNEZ R1 Loop

Register result status		F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1								
18	56 Qi	Mult1							

Loop Example Cycle 19

Instruction status				Execution			Write			
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address		
LD	F0	0 R1	1	1	9	10	Load1	No		
MULTI	F4	F0 F2	1	2	14	15	Load2	No		
SD	F4	0 R1	1	3	18	19	Load3	Yes	64	Qi
LD	F0	0 R1	2	6	10	11	Store1	No		
MULTI	F4	F0 F2	2	7	15	16	Store2	Yes	72	M(72)*R(
SD	F4	0 R1	2	8			Store3	Yes	64	Mult1

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes	MULTD	R(F2)	Load3		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status		F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1								
19	56 Qi	Mult1							

Loop Example Cycle 20

Instruction status				Execution			Write			
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result	Busy	Address		
LD	F0	0 R1	1	1	9	10	Load1	No		
MULTI	F4	F0 F2	1	2	14	15	Load2	No		
SD	F4	0 R1	1	3	18	19	Load3	Yes	64	Qi
LD	F0	0 R1	2	6	10	11	Store1	No		
MULTI	F4	F0 F2	2	7	15	16	Store2	Yes	72	M(72)*R(
SD	F4	0 R1	2	8	20		Store3	Yes	64	Mult1

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	V _j	V _k	Q _j	Q _k	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes MULTD		R(F2)	Load3		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status		F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1								
20	56 Qi	Mult1							

Loop Example Cycle 21

Instruction status				Execution			Write		Busy Address	
Instruction	<i>j</i>	<i>k</i>	iteration	Issue	complete	Result				
LD	F0	0 R1	1	1	9	10	Load1	No		
MULTI	F4	F0 F2	1	2	14	15	Load2	No		
SD	F4	0 R1	1	3	18	19	Load3	Yes	64 Qi	
LD	F0	0 R1	2	6	10	11	Store1	No		
MULTI	F4	F0 F2	2	7	15	16	Store2	No		
SD	F4	0 R1	2	8	20	21	Store3	Yes	64 Mult1	

Reservation Stations			S1	S2	RS for <i>j</i>	RS for <i>k</i>	Code:
Time	Name	Busy Op	<i>V_j</i>	<i>V_k</i>	<i>Q_j</i>	<i>Q_k</i>	
0	Add1	No					LD F0 0 R1
0	Add2	No					MULTI F4 F0 F2
0	Add3	No					SD F4 0 R1
0	Mult1	Yes MULTD		R(F2)	Load3		SUBI R1 R1 #8
0	Mult2	No					BNEZ R1 Loop

Register result status		F0	F2	F4	F6	F8	F10	F12...	F30
Clock	R1								
21	56 Qi	Mult1							

Tomasulo Summary

- Prevents Register as bottleneck
- Avoids WAR, WAW hazards of Scoreboard
- Allows loop unrolling in HW
- Not limited to basic blocks (provided branch prediction)
- Lasting Contributions
 - Dynamic scheduling
 - Register renaming
 - Load/store disambiguation
- Next: More branch prediction